고객 승인원 관리대장

개정번호	개정일자	개정 Page	개정이력	담당자	비고
00	2016.06.14	1~12	신규 제정	박주용	
01	2017.08.28	1~13	Chip Diagram 및 분류기준 변경	강민우	

1B-25, 727, Wonsi-dong, Danwon-gu, Ansan-city, Gyeonggi-do, Korea 425-851

Customer: Seoul Semiconductor Co., Ltd.

Part Name: UW1111-EB-39 (395nm)

Contents:

Seoul Viosys Co., Ltd.		
Drawn by	Checked by	Approved by
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17/08/28	17/08/28	17/08/28

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Checked by		Approved by

1. Features and Application

- High Luminous Intensity, Long Operation Life
- Package-less module

2. Part Name:

- UW1111-EB-39

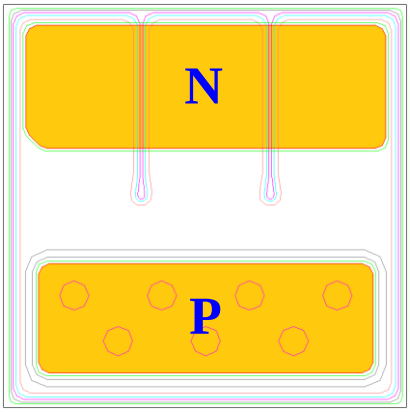
3. Main Material

- Substrate: Al_2O_3 (Sapphire)
- Epitaxial Layer: GaN Based LED Structure

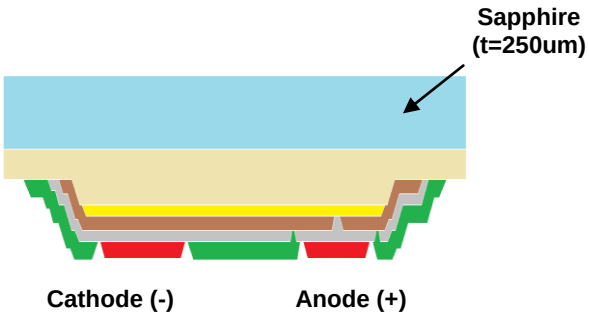
4. Electrodes

- P-Electrode: Au alloy
- N-Electrode: Au alloy

5. Chip Diagram



<Fig. 1 >Plane View



<Fig. 2> Cross Sectional View

6. Maximum Ratings

Item	Symbol	Value	Unit
DC forward current (Ta=25℃)	I_f	700	mA
Pulsed forward current [a] (Ta=25℃)	I_{fp}	1000	mA
Junction temperature [b]	T_j	125	˚C
Operating Temperature Range	T_{op}	-30 to + 85	˚C
Storage Temperature Range	Tst	-40 to +100	˚C

Note. 'Maximum Ratings' mean when it exceeds the chip has the possibility of breaking down when these conditions are exceeded momentarily. 'Maximum ratings', the chip is not guaranteed to endure such conditions. 'Maximum Ratings' concerning your LED device after the chip is built into your package shall be established by yourself since these greatly depend on the design of the device, the conditions of assembly, the environment used, and so forth.

[a] 1/10 Duty , f=1kHz

[b] Measurement condition ; Metal Core PCB

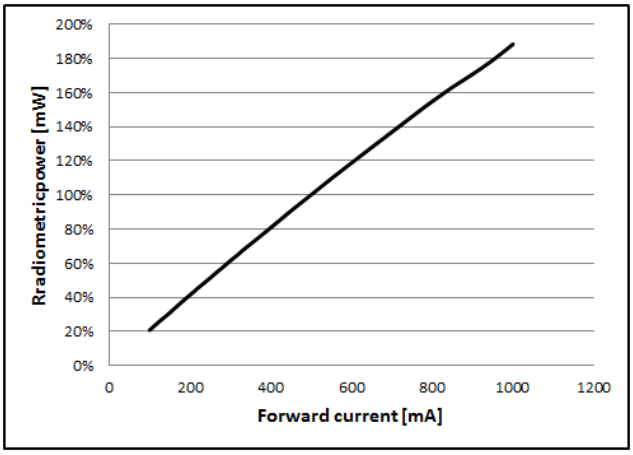
7. Typical Electro-Optical Characteristics at Ta=25℃

Item	Symbol	Condition	Characteristics (Ta=25℃)			Unit
			Min	Typ	Max	
Reverse Current	I_R	V_R =-5V	0	-	1.0	uA
Turn-on Voltage	V_{F1}	I_F =1 μA	2.0	-	3.0	V
Forward Voltage	VF	I_F =500mA	3.3	-	3.6	V
Peak Wavelength [1)]	λ_d	I_F =500mA	390		400	㎚
Full Width Half Maximum	Δλ	I_F =500mA	-	12	-	㎚
Radiant Power [2)]	Po	I_F =500mA	750	825	870	mW

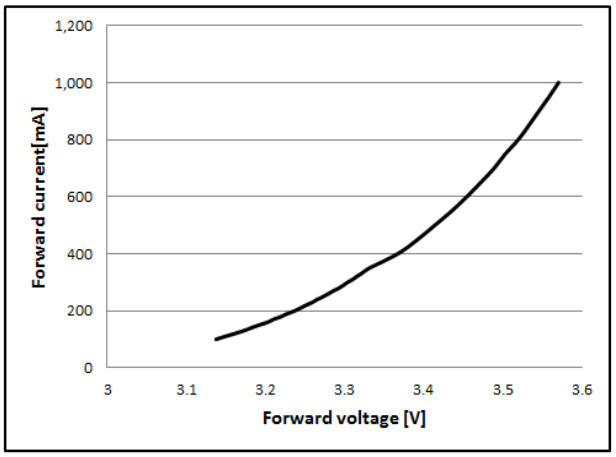
Note: Radiant and Peak wavelength are measured by Seoul Viosys' equipment. (*1, *2)

Peak Wavelength: ±1nm. (*1)

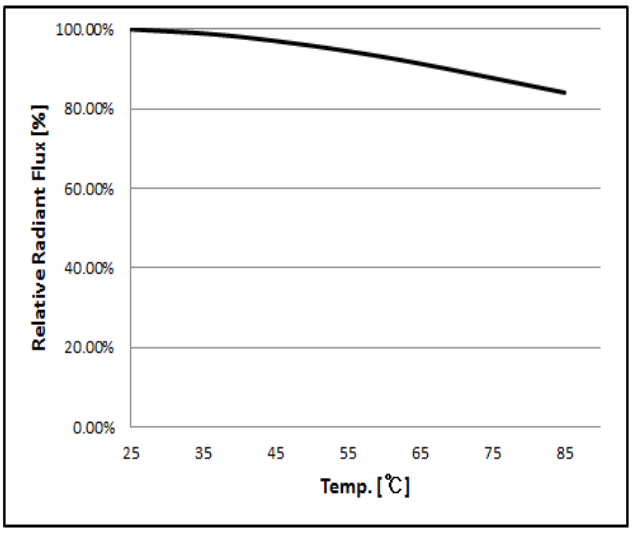
Radiant Power : ±10%. (*2)



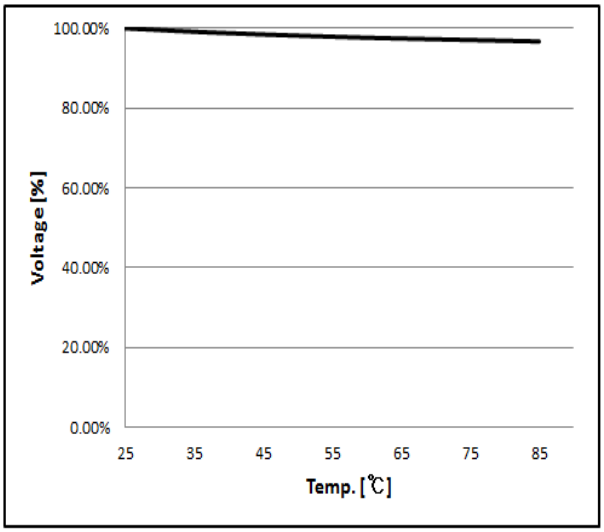
Forward Current vs. Light Output



Forward Voltage vs. Forward Current



Temperature vs. Relative Radiant Flux



Temperature vs. Relative Forward Voltage

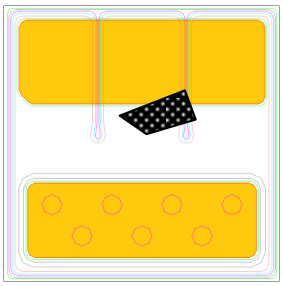
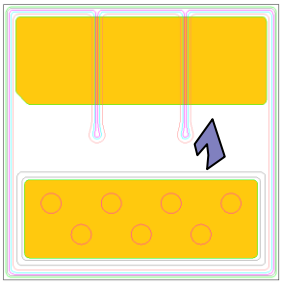
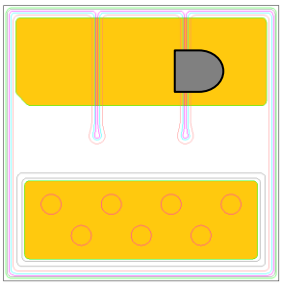
8. Mechanical Specifications

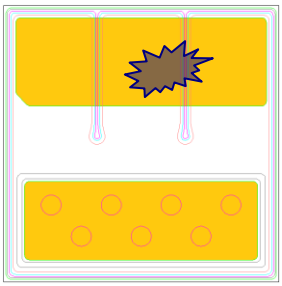
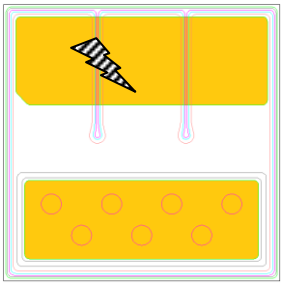
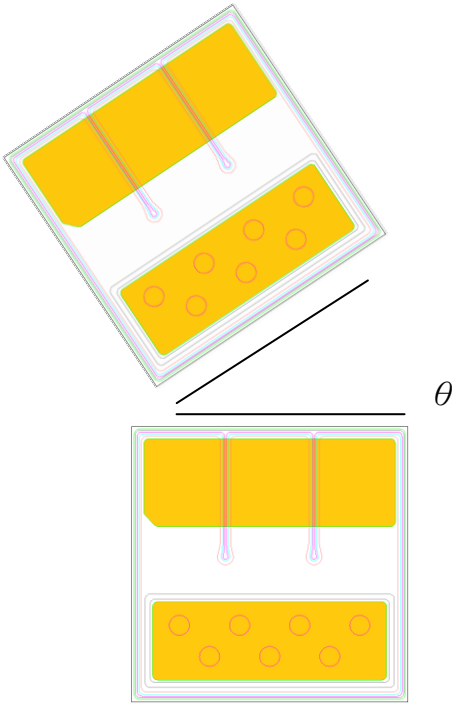
(Unit: ㎛)

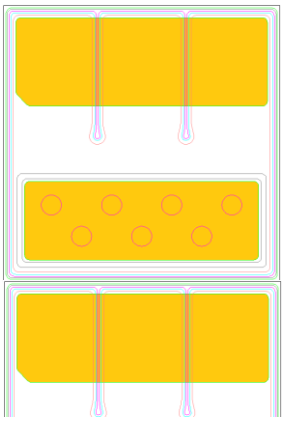
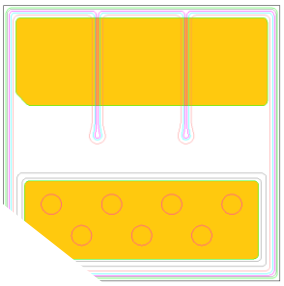
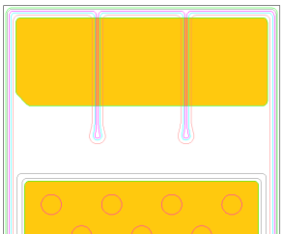
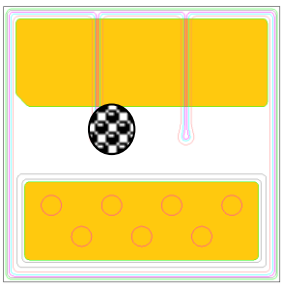
Description	Dimension	Tolerance
Top emitting area	1100um x 1100um	±40
Bottom substrate	1100um x 1100um	±40
Chip Thickness	250um	±15
P-Pad Diameter	913um x 299um	±50
N-Pad Diameter	983um x 337um	±50

9. Visual inspection

Done by optical microscope (20x).

Item	Accepted (OK)/defective (N.G.)	Example
Surface dirt	accepted : if surface dirt(metal) less than 20% of chip	
Passivation film peeling	accepted : if Passivation film peeling less than 30% of chip.	
Partially missing pad	accepted : a < b/5 a: missing bond pad b: normal bond pad	

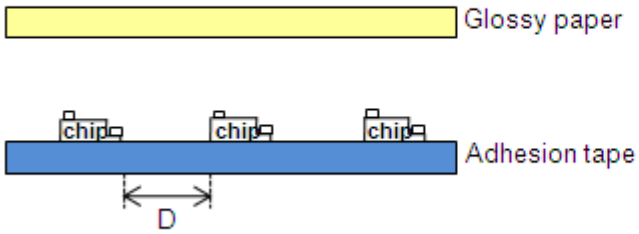
Metal peeling	rejected : if Metal peeling more than 20% of chip area.	
Bond pad scratch	accepted : if bond pad scratch (including probe mark) less than 20 % of chip area.	
θ shift	accepted : θ < ±5°	

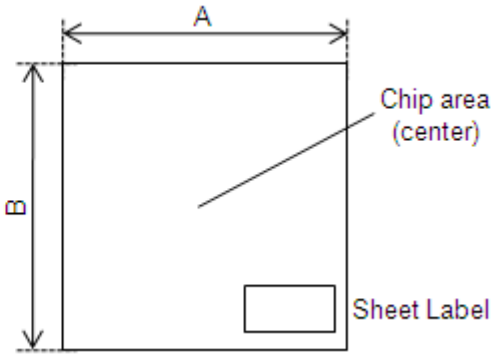
Twins or triples	Inseparable chips are rejected If extra-size is less than 10%, OK.	
Chipping	Pad electrode not chipped off	
Bad cut	Not accepted : if bad cut is occurred	
Pinholes	accepted : if pinhole less than 20% of chip	

10. Packing

(1) Chips on tape

(a) Electro-Optical measurement data should be labeled and tacked on the backside of the glossy paper. Chip area should be placed in the center of adhesion tape, and the wire-bonding pad should face towards the covered glossy paper.





(b) Chip type, Lot No. and quantity etc. should be labeled and tacked to the corner of the glossy paper.

Item	Instruction
Adhesion tape	Semi- transparent blue
Glossy paper (A×B)	197mm × 220mm
Chip Qty tape	Typ. 2,000ea
Chip separation (D)	D : 0.40mm

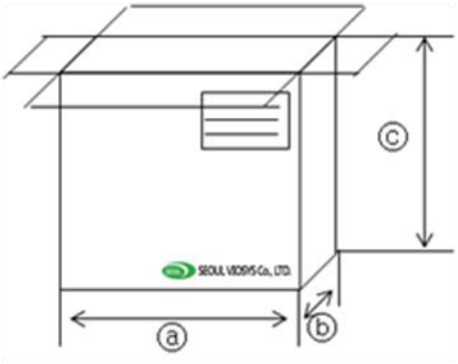
(2) Packing for shipment

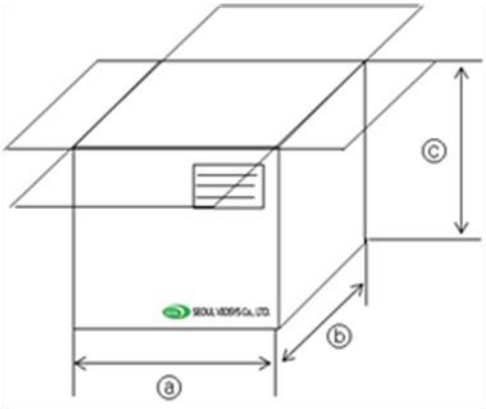
(a) The sheets (adhesion tape + glossy paper) are packed in an anti-static electricity bag. Each anti-static bag can contain up to 20 sheets.

(b) The anti-static bags are packed in a box. The size of this box is 250mm×65mm×275mm (ⓐ × ⓑ × ⓒ). Each box can contain up to 5 anti-static electricity bags.

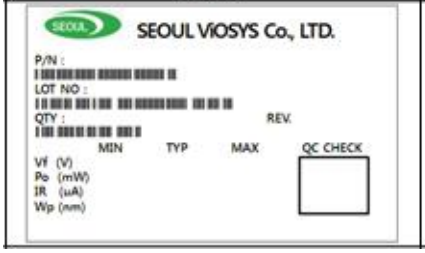
(c) The boxes which contain anti-static electricity bags are packed in the other box. The size of this outer box is 260mm×340mm×290mm (ⓐ × ⓑ × ⓒ). Each outer box can contain up to 5 inner boxes.

(d) Each sheet / box is labeled with information describing its content. (Details please refer to section 12)





11. Labeling

Sheet	Inner Box	Outer Box
		

(1) Sheet : The measurement data for each lot are also shown on the backside of the sheet.

(2) Inner Box : The information about the products is also shown on the inner box.

(3) Outer Box : The information about the products is also shown on the outer box.

12. Precaution

(1) Quality Guarantee

The chip guarantee period is three months after the delivery under the following preservation conditions. If any defective is found, the customer shall immediately inform of that to Seoul Viosys Co., Ltd. Preservation conditions (when the shipping package is unopened.)

· Temperature: 0 ~ 60 ˚C

· Atmosphere: Keep the chips in a desiccator with silica gel or with nitrogen substitution.

(2) General precautions for use

· Chips should be stored in a clean environment. If the Chips are to be stored for 3 months or more after being shipped from Seoul Viosys, they should be packed by a sealed

container with nitrogen gas injected.
(Shelf life of sealed bags : 1year, 0~40˚C of temperature , 20~70% of RH)

· This chip should not be used directly in any type of fluid such as water, oil, organic solvent, etc. When washing is required, IPA is recommended to use.

· After storage bag is open, device subjected to soldering, solder flow, or other high temperature processes must be:
Mounted within 168 hours (7days) at an assembly line with a condition of no more than 30˚C and 60% RH

· Chips require baking before mounting, if humidity card reading is >60% at, 23.5˚C. chips must be baked for 24Hrs. at 65.5˚C, if baking required.

· When the chips are illuminating, the maximum ambient temperature should be first considered before operation. If voltage exceeding the absolute maximum rating is applied to chips, it may cause damage or even destruction to chips. Damaged LEDs will show some abnormal characteristics such as remarkable increase of leak current, lower turn-on voltage and getting unlit at low current.

· The appearance and specifications of the products may be modified for improvement without further notice.

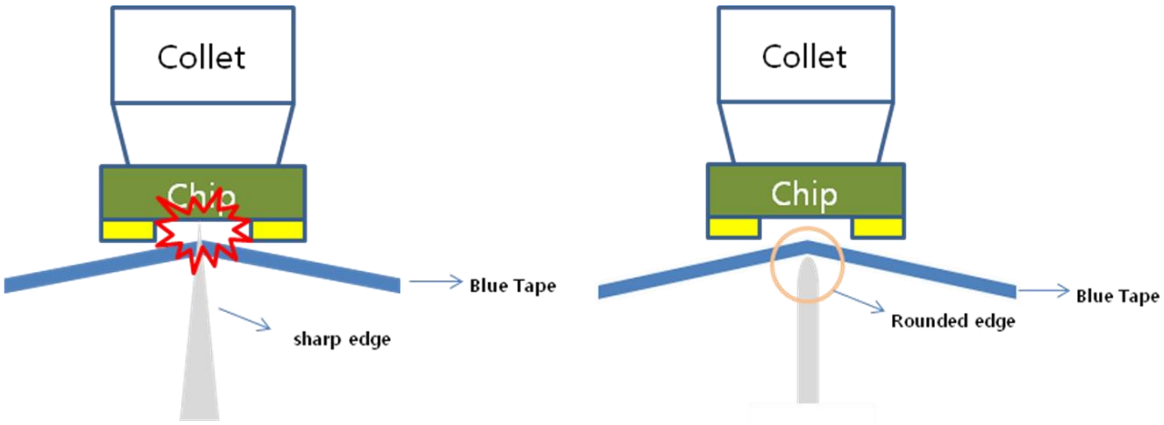
· The chips are sensitive to the static electricity and surge. It is strongly recommended to use a grounded wrist band and anti-electrostatic glove when handling the LEDs.

(3) Precautions for Die Attach (Pick and Place)

· Unlike the top of chip, the bottom (The opposite side of sapphire substrate) is the

epitaxial Layer where the p-n junction is located. It is not mechanically protected and can be damaged if a sharp and hard ejector pin material is used.

· Seoul Viosys recommends an ejector pin with rounded edge to minimize the risk of mechanical damage.



(a) (b)

(a) Sharp ejector pin tip may damage the Flip Chip (left). (b) A rounded tip minimizes the risk of damage caused by ejector pin (right).

The above specifications are subject to change with prior notice.

Seoul Viosys Co., Ltd

Aug 28th, 2017